

## CLAIM LISTING

1-17. (Cancelled)

18. (Currently Amended) A direct memory access controller, said direct memory access controller comprising:

a state logic machine for receiving a single command to provide a specified ~~selectable~~ range of a plurality of sequential data words, wherein the single command expressly states a starting address and an ending address of said specified range; and

a memory controller for fetching a first portion of the specified selectable range and a second portion of the specified selectable range after fetching the first portion, wherein the second portion of the range has a lower address than the first portion, after the state logic receives the single command including the starting address and the ending address.

19. (Previously Presented) The direct memory access controller of claim 18, wherein the memory controller fetches the first portion of the range and the second portion of the range in a forward address order.

20. (Previously Presented) The direct memory access controller of claim 18, further comprising:

a local buffer for storing the first and second portions in a forward address order, said local buffer comprising a plurality of data words.

21. (Previously Presented) The direct memory access

controller of claim 20, wherein the plurality of data words of the local buffer are narrower in width than the sequential data words.

22. (Previously Presented) The direct memory access controller of claim 20, further comprising:

a port for transmitting the contents of the plurality of data words of the local buffer in a reverse address order.

23. (Previously Presented) The direct memory access controller of claim 22, further comprising:

at least one multiplexer for reversing the bit positions of contents of at least one of the data words of the local buffer.

24. (Currently Amended) A method for fetching data words, said method comprising:

receiving a single command to provide a ~~specified~~ ~~selectable~~ range of a plurality of sequential data words in a memory, wherein the command expressly states a starting at a beginning address and ending at an ending address of said range;

fetching a portion, in a forward address order, of the range of sequential data words, said wherein said portion of the range of sequential data words consists of a predetermined amount of data words that conclude with and precede the ending address, and wherein the predetermined amount of data words is equivalent to a capacity of a local buffer;

storing the predetermined amount of data words that conclude with and precede the ending address in the

local buffer;

fetching, in the forward address order, at least one preceding portion of the range of sequential data words, wherein each of the preceding portions of the range of sequential data words consist of the predetermined amount of data words; and

wherein a one of the preceding portions of the range of sequential data words comprises the starting ~~beginning~~ address, truncating those data words that precede the beginning address.

25. (Previously Presented) The method of claim 24, further comprising:

loading the portion and the at least one preceding portions of the sequential data words into the local buffer.

26. (Previously Presented) The method of claim 25, further comprising:

reversing the portion and the at least one preceding portions of the range of sequential data words.

27. (Previously Presented) The method of claim 26, further comprising:

reversing the truncated one of the preceding portions of the range of sequential data words that comprises the beginning address.

28. (Previously Presented) The direct memory access controller of claim 18, wherein the first portion and the second portion are adjacent to each other.

29. (Previously Presented) The direct memory access controller of claim 18, wherein the specified selectable range of the plurality of sequential data words is less than a memory storing the plurality of sequential data words.

30. (New) A system for decoding video data, said system comprising:

- a memory for storing a packetized elementary stream, said packetized element stream comprising a plurality of packets;

- a start code table for storing starting addresses and ending addresses of said plurality of packets;

- a video decoder for decoding a particular one of the plurality of packets, wherein the video decoder looks up the starting addresses and the ending addresses of the particular one of the plurality of packets and issues a single command to fetch the packet, wherein the single command expressly includes a starting address and an ending address associated with the particular one of the plurality packets; and

- a direct memory access controller, said direct memory access controller comprising:

  - a state logic machine for receiving the single command; and

  - a memory controller for fetching a first portion of a range, said range comprising sequential data words from the starting address to the ending address for the particular one of the plurality of packets, and a second portion of the range after fetching the first portion, wherein the second portion of the range has a lower address than the first portion, after the state logic receives the

single command including the starting address and the ending address.